CLAIMS

What is claimed is:

1. A semiconductor die package, comprising:

conductive outer leads having first ends extending outside the package and second ends extending toward the interior of the package;

conductive inner leads having first ends extending to and electrically accessible through a first surface of the package; and

a first die electrically connected to the inner and outer leads.

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2. The package of Claim 1, wherein the first ends of the outer leads do not extend beyond the first ends of the inner leads.

3. The package of Claim 1, wherein the first ends of the outer leads extend beyond the first ends of the inner leads.

4. The package of Claim 1, wherein the first surface is a bottom surface.

5. The package of Claim 4, further comprising a printed circuit board electrically coupled to the outer and inner leads.

6. The package of Claim 4, wherein the first ends of the inner leads are approximately co-planar with the first ends of the outer leads.

7. The package of Claim 4, wherein the first die is positioned above the inner leads.

8. The package of Claim 1, wherein the first surface is an upper surface.

9. The package of Claim 8, wherein the first die is positioned between the outer leads and the inner leads.

10. The package of Claim 8, further comprising a second semiconductor die package coupled to the first die, wherein the second semiconductor die package comprises a second die and outer leads coupled to the second die.

11. The package of Claim 10, wherein the outer leads of the second die are electrically coupled to the inner leads of the first die.

12. The package of Claim 11, wherein the second die package is positioned over the first die.

13. The package of Claim 1, wherein the inner leads further comprise an interior portion electrically accessible through the first surface, and wherein the die is further electrically coupled to the interior portion.

14. The package of Claim 13, wherein the interior portion and the first ends of the inner leads and the

first ends of the outer leads are electrically coupled to a printed circuit board.

15. A semiconductor die package, comprising:

a plurality of conductive outer leads having first and second ends, wherein the first ends extend outside the package;

an internal paddle area comprising conductive inner leads having first ends, wherein the first ends of the inner leads are electrically accessible through a surface of the package;

a die attached to the internal paddle area;

first wires coupling the die to the outer leads; and

second wires coupling the die to the inner leads.

16. The package of Claim 15, wherein the surface is a bottom surface.

17. The package of Claim 15, wherein the surface is an upper surface.

18. The package of Claim 15, wherein the first ends of the inner leads are closer to the die than the first ends of the outer leads.

19. The package of Claim 15, wherein the first ends of the inner leads extend beyond the second ends of the outer leads.

20. The package of Claim 15, wherein the first ends of the inner leads do not extend beyond the second ends of the outer leads.

21. The package of Claim 15, wherein the internal paddle area has an interior conductive portion electrically accessible through the surface of the package.

22. A method of forming a semiconductor die package, the method comprising:

providing a lead frame having external leads and an internal paddle area with slots and electrically coupled traces;

securing the internal paddle area;

removing outer portions of the paddle area to electrically isolate the traces and create internal leads from the traces;

bending ends of the internal leads towards a surface of the package; and

encapsulating the internal paddle area, wherein the ends of the internal leads are electrically accessible through the surface of the package.

23. The method of Claim 22, wherein the ends are bent towards a bottom surface of the package.

24. The method of Claim 22, further comprising, prior to the encapsulating:

attaching a die to the internal paddle area;

electrically coupling the die to the external leads; and

electrically coupling the die to the internal leads.

25. The method of Claim 23, further comprising electrically coupling the external and internal leads to a printed circuit board.

26. The method of Claim 22, wherein the ends are bent towards a top surface of the package.

27. The method of Claim 26, further comprising placing a second die package over the die package and electrically coupling the internal leads to a die contained within the second die package.

28. A method of forming a semiconductor die package, the method comprising:

providing a lead frame having internal and external leads electrically coupled together at first portions of the lead frame, the ends the internal leads extending beyond the ends of the external leads;

securing the internal leads;

removing the first portions;

bending the ends of the internal leads towards a surface of the package; and

encapsulating the package, wherein the ends of the internal leads are electrically accessible through the surface of the package.

29. The method of Claim 28, wherein the ends are bent towards a lower surface of the package.

30. The method of Claim 28, wherein the ends are bent towards an upper surface of the package.

31. The method of Claim 28, further comprising, prior to the encapsulating:

attaching a die to the lead frame;

electrically coupling the die to the external leads; and

electrically coupling the die to the internal leads.

32. The method of Claim 28, wherein the securing comprises placing a tape on the internal leads.